International Journal of Applied Information Systems (IJAIS) – ISSN : 2249-0868
Foundation of Computer Science FCS, New York, USA
Volume 10 – No.7, March 2016 – www.ijais.org

A Novel High-speed Adder-Subtractor Design based on CNFET

Shimaa I. Sayed
Electronics, Communication, and Computer
Helwan University
Egypt

Salah El-Din H. Gamal
Department of Physics and Mathematics
Ain Shams University
Egypt

ABSTRACT
Carbon Nanotube filed-effect transistor (CNFET) is one of the promising alternatives to the MOS transistors. The geometry-dependent threshold voltage is one of the CNFET characteristics, which is used in the proposed design. In this paper, we present a novel high speed Adder-subtractor cell using CNFETs based on XOR gates and multiplexer. Presented design uses fourteen transistors, ten for full adder and four to modify the cell for subtraction. Simulation results show significant improvement in terms of delay and area saving with 48% and 11% respectively compared to the latest design. Simulations were carried out using HSPICE based on CNFET model with optimized design parameters.

Keywords
Single walled CNT, Adder-Subtractor, High speed, and Digital electronics.

1. INTRODUCTION
Full-adder cells are one of the fundamental parts of digital circuits. By putting them together and wiring these cells in the correct way arithmetic circuits like addition, multiplication, division, exponentiation, etc. can be achieved [1, 2].

Various full-adder circuit designs have been proposed by many researchers [3-6]. Implementation of the most full-adder designs has been done by conventional CMOS technology. Nowadays, as the dimensions decreased to nano ranges, designing digital circuits using CMOS technology faced many difficulties such as leakage current in short channel nanometer transistors. It has several types, such as reverse biased diode leakage, subthreshold leakage, gate oxide tunneling current, hot carrier gate current, gate induced drain leakage and channel punch-through current [7-10]. Because of the limitation of CMOS technology, it is gradually replaced by new technologies and devices that are the achievement of nanotechnology such as Carbon Nanotube Field Effect Transistor (CNFET).

CNFET is one of the several cutting-edge emerging technologies within nanotechnology with high efficiency and a wide range of applications in many different streams of science and technology. Nano-circuits which are based on carbon nanotubes such as CNFETs show big promise of less delay and power consumption than available silicon-based FETs. Many works and circuit designs through CNFET have been proposed by CNFET researchers [11-14]. The proposed high speed full-adders based on CNFETs which are mentioned in [15] and [16], presented the full-adder circuits by the combination of the majority-not and capacitors. Using capacitors to present expected behavioral Full Adder, will increase the delay, chip area and also less noise margin.

In this paper, the simulation results demonstrate that our proposed adder-subtractor design has better performance compare to the previous work. The rest of this paper is organizes in this way: CNFETs are briefly reviewed in the next section. In section III the chosen parameters will be presented to optimize the performance of CNFET. Following with section IV, the discussion of the full adder cell of previous work including its advantages and disadvantages then new proposed adder-subtractor cell is presented. The simulation results of the novel high speed full adder based-on CNFET with detailed description provided in section V. Finally, conclusions and remarks are reported.

2. REVIEW OF CNFET
Carbon Nano-Tube (CNT) has attracted attention in recent years not only for its relatively small dimensions and near ballistic transport, but also for its potential of implementations in many digital circuits. CNFETs use semi conducting single wall carbon nanotube (s-SWCNT) as transistor channel. Two types of CNFET, based on connection between s-SWCNT and source/drain of transistor are presented. If a s-SWCNT directly contact to source and drain of transistor, Schottky barrier transistor is created in their junction. The disadvantage of Schottky barrier CNFET (SB-CNFET) is that Ion/Ioff ratio is low. MOSFET like CNFET is another type of CNFET which unlike SB-CNFET exhibit ambipolar behaviors. This type of CNFET is doped in un-gated portions and behaves like MOSFET transistor. MOSFET like CNFETs have good characteristic such as; scalability compared to SB-CNFET, reduced off leakage current and high current in source to channel junction in absence of Schottky barrier. Depending on the rolling up of the CNT, SWCNFET can act as conductor or semiconductor. This property which is determined with the chirality vector is represented by integer pair (n1, n2). Diameter of SWCNT with this vector is calculated using the following formula.

$$D_{CNT} = \frac{a\times\sqrt{n_1^2+n_2^2+n_1n_2}}{\pi} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1n_2} \quad (1)$$

Where ‘a’ is the lattice constant which is equal to 2.49. Threshold voltage is the voltage required to turn transistor on. Threshold voltage of CNFET transistors is dependent on diameter of SWCNT that is used in channel of transistor. The CNFET threshold can be calculated by (2) below.

$$V_{th} \approx \frac{0.43}{D_{CNT\ (nm)}} \quad (2)$$

This formula determines that CNTFETs turn on according to their CNT diameter in various voltages. This formula shows that the CNFET turns on at different voltages depending on their diameters. This practical characteristic makes CNFET more flexible than MOSFET for designing digital circuits and makes it very suitable for designing multi-V_{th} circuits. The CNFET has many design parameters such as operating voltage, number of

tubes, pitch, nanotube diameter, dielectric constant and contact materials which determine the digital circuit performance. This paper proposes a new CNFET design parameters to optimize performance characteristics such as delay, power consumption and area for designing Adder-subtractor cell.

3. OPTIMIZATION OF PURE-CNFET PARAMETERS

In CNFETs one or more semiconducting SWCNTs are used as the channel of the device. Fig. 1 shows the schematic of a typical CNFET device. The distance between the centers of two adjacent SWCNTs under the same gate of a CNFET is called pitch (S), which directly impacts I_{on}/I_{off} ratio. The width of the gate of a CNFET (W) can be approximately calculated based on the following equation.

$$W= (N-1)S+D_{CNT} \quad (3)$$

Where N is the number of nanotubes under the gate and D_{CNT} is the diameter of carbon nanotube. It is important to determine the number of CNTs to be used in an array in order to ensure sufficient current supply for driving fixed capacitive loads. It is worth noting that the total current drive in a CNFET depends on the number of CNTs per device. This explains the increase in current driving capability of the device with increasing the number of CNTs. However, increase in number of CNT also incurs penalty in power dissipation and area. We conclude that the upper limit on the number of CNTs used is determined by the power-performance trade-off but still looking at the overall performance merits obtained.

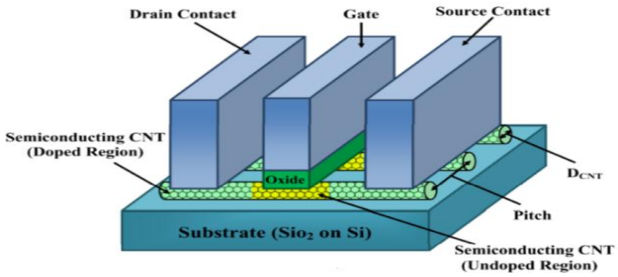

Fig 1: Schematic diagram of a CNFET device

To maximize circuit performance at the 32 nm node, the number of carbon nanotube chosen to be 8. The second parameter is inter-nanotube spacing (Pitch), the drain current of the CNFET is dependent on pitch value which determines the amount of screening effect. The I_{on}/I_{off} can be enhanced by increasing the pitch due to weakening the charge screening effect. However a larger pitch degrades the integration density. The trade-off between I_{on}/I_{off} and area efficiency lead to choose optimum pitch equal to 10nm. The third parameter is dielectric material and its thickness. To improve the device performance further, a thinner gate insulator with a higher dielectric constant can be used. Recently, high dielectric material such as ZrO_2 thin film has been employed in top-gated CNFETs as the insulator with thickness 2.5nm. The final parameter is a contact material, the contact between semiconducting CNT (s-CNT) and metal is generally modeled as a Schottky barrier, resulting from the Fermi level mismatch between s-CNT and metal electrode. Palladium (Pd), which is a noble metal with high work function and good wetting interactions with CNT, has been found with good electrical contact to both semiconducting and metallic CNTs.

4. PROPOSED FULL ADDER-SUBTRACTOR

Our proposed adder-subtractor depends on implementing adder with high performance included in high speed, less area and good in voltage swing. Some modifications applied on adder cell to operate as adder or subtractor with control line. The design based on XOR and multiplexer implemented by Pass Transistor Logic (PTL).

4.1 Full Adder Cell

There are some implementations of various full-adder cell designs based CNFET. The full adder design mentioned in [17] is used in this paper for comparison after applying optimized parameters. Ultra-Low Power and High Speed Full Adder is presented. The main idea of their design is implementing Equ(4) for calculating sum and Equ(5) for calculating carry. Transistor level of this adder cell is shown in Fig. 2. In this cell they have two levels for computing either sum or carry. They need eight CNT transistors to implement sum and six CNT transistors to implement carry which four of them have been shared in both (Sum and Carry) circuit design so the total number of transistors which are required for the adder is ten. The logic function of the output and the carry could be described by the following equations.

$$Sum = (A \oplus B) \oplus Cin$$
$$= (A \oplus B)Cin` + (A \oplus B)`Cin \quad (4)$$

$$Carry = AB + BCin + CinA$$
$$= (A \oplus B)`A + (A \oplus B)\,C\text{in} \quad (5)$$

The main idea of this design is using beneficial characteristics of CNFET to solve the voltage swing problem. It can be control threshold voltage of CNT transistor by changing the diameter of CNT. Thus reducing the threshold voltage by increasing the diameter of CNT could solve the threshold loss problem.

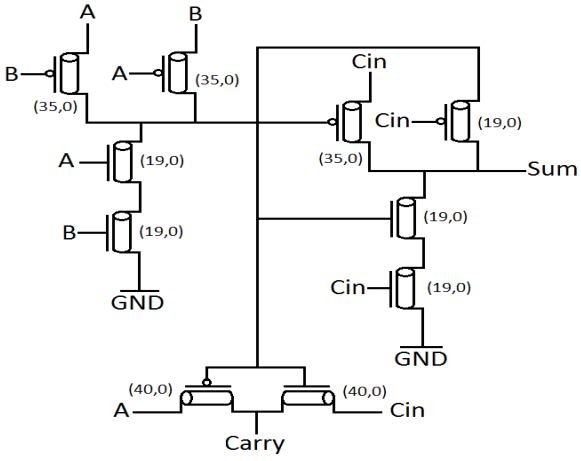

Fig.2: Schematic diagram of full adder cell based on CNFET

In this design, we combine between beneficial characteristics of CNFET and using optimized parameters of CNFET. By the first, increasing the diameter of CNT could solve the threshold loss problem. Thus the voltage swing problem related to the output node of the full adder cell is solved. The second idea is choosing the best design parameters of CNFET and applying it to the same circuit. These parameters lead to reducing delay and minimizing the area required by the transistors. These benefits included in our adder-subtractor design which make it efficient

for digital design. Regarding to the simulation results, we have impressive improvement in term of delay and area saving compared to the CNFET implementation in [17].

4.2 Adder/subtractor cell

A binary adder-subtractor is a combinational circuit that performs the arithmetic operation of addition and subtraction with binary numbers. In our proposed design, we developed the full adder cell to operate as an adder or a subtractor. The main idea of our design is implementing multiplexer made of Two pass transistors to choose one among two as shown in Fig. 3.

The control line of the multiplexer called the mode M which controls the operation of the adder-subtractor cell. The adder-subtractor cell operates according to the input M. When M=0 the multiplexer select the input B to added with input A so, the circuit performs an addition operation. When M = 1, the circuit add input A and complement of B with one so, it becomes a subtractor. By connecting n-blocks such one-bit Full adders, n-bit ripple adder can be obtained.

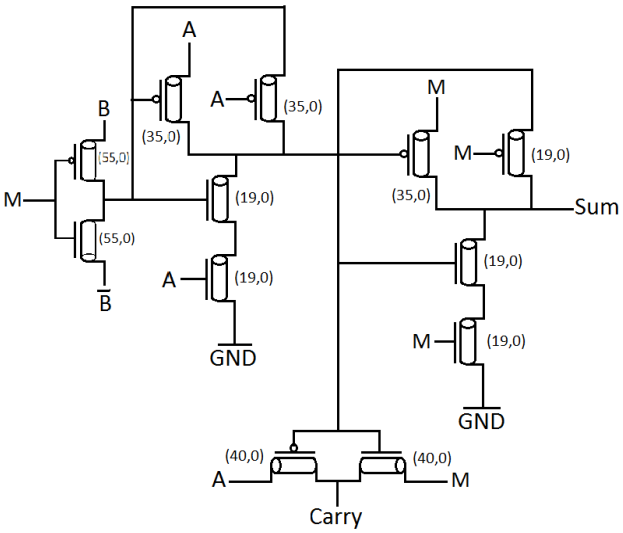

Fig 3: Schematic diagram of proposed adder-subtractor cell based on CNFET

5. SIMULATION RESULTS

In this section, the modified full adder design is compared with the latest full adder design by CNFET [17]. The circuits are simulated at room temperature and the supply voltage is 0.6V. All designs are simulated at 32nm CNFET with HSPICE. To verify the output functionality of the novel high speed adder-subtractor circuit, Transient response of the design viewed in Fig. 4. It shows the outputs of bit full adder cell which is completely full swing.

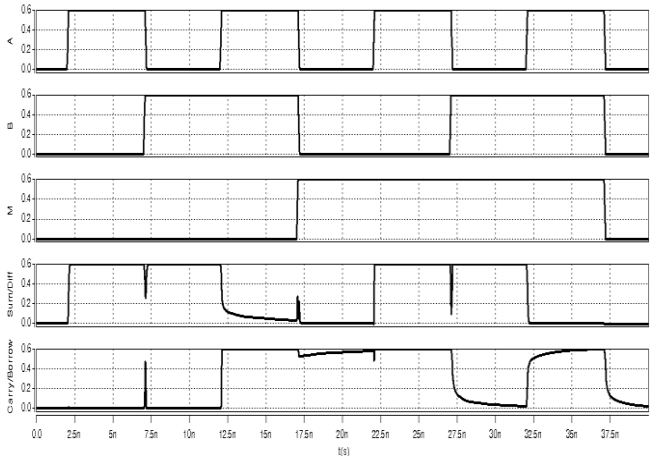

Fig 4: Transient response of proposed adder-subtractor cell design.

To compare these adders, power dissipation, delay and width of CNFET are evaluated. Table1 shows the comparison of simulation results between CNFET adder with non-optimized and optimized parameters.

Table 1. Bit Full Adder Comparison with f=100mhz & cl=3.5ff

	F=100MHz Cl=3.5fF at 30ns trans time		
	Power (E-08) W	***Delay (E-11) S***	***Width of CNFET (nm)***
CNFET adder presented in [17]	3.0522	1.1180	90
CNFET adder presented in [17] with optimized parameters	3.0587	0.3979	80

The obtained speed up for optimized circuit is 64% in comparison with [17]. According to the width of CNFET, the proposed optimized adder saves 11% in the required area with the same power consumption.

Table2 shows simulation results of a novel adder-subtractor cell with default and optimized parameters. It improves the speed by 48% and saves the area by 11% compared with the same design with N=3 and S=30nm. Consequently, the speed up of proposed design cell is better than any adder-subtractor cell.

TABLE 2. Bit Full Adder-Subtractor Comparison with f=100mhz & cl=3.5ff

	F=100MHz Cl=3.5fF at 30ns trans time		
	Power (E-7) W	***Delay (E-11) S***	***Width of CNFET (nm)***
Proposed Adder-subtractor with N=3, S=30	0.877	7.7719	90
Proposed Adder-subtractor with optimized parameters	1.0339	4.0128	80

In order to compare more precisely, proposed design is also simulated in different load capacitance as shown in Fig.5. As the load capacitance increases, the delay of the adder-subtractor increases. But the improvement of the speed up for our design is enhanced. Therefore, results show that the proposed adder-subtractor cell has better performance in all situations.

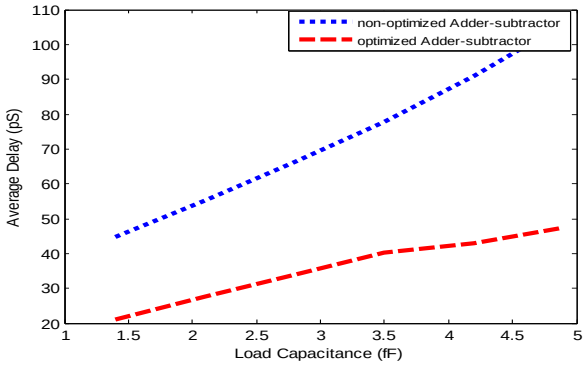

Fig. 5 Average delay of Adder-subtractor cell in different load capacitance

6. CONCLUSION

In this paper, an improved performance of CNFET Full Adder cell with ten transistors has been presented. The significant improvement is achieved by applying optimized parameters which results in reduction in the delay and area required by CNFET. After that, a novel adder-subtractor design is proposed using CNFET based on XOR gates and multiplexer. Presented design has less number of transistors with high performance for digital circuit design. The simulation results show that on average, speed enhancement and area saving of 48% and 11% can be achieved with optimized parameters design over default values of these parameters. The cumulative benefits of the novel adder-subtractor design based CNFET result in an PDP reduction by a factor of 41%.

7. REFERENCES

[1] N. Weste, K. Eshragian, "Principles of CMOS VLSI Design: A Systems Perspective", Addison-Wesley, 1993.

[2] R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic", Solid-State Circuits, IEEE Journal of. 32 (7) (1997) 1079–1090.

[3] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, O. Kavehei, "A novel low power full-adder cell for low voltage", Integration, the VLSI Journal, Elsevier 42 (4) (2009) 457–467.

[4] K. Navi, V. Foroutan, M. Rahimi Azghadi, M. Maeen, M. Ebrahimpour, M. Kaveh, O. Kavehei, "A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter", Microelectronics Journal, Elsevier 40 (10) (2009) 1441–1448.

[5] K. Navi, M.H. Moaiyeri, R. Faghih Mirzaee, O. Hashemipour, B. Mazloom Nezhad, "Two new low-power full Adders based on majority-not gates", Microelectronics Journal, Elsevier 40 (2009) 126–130.

[6] K. Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, N. Dadkhahi, "Low power and high-performance 1 bit CMOS full-adder cell", Journal of Computers. 3 (2) (2008) 48-54.

[7] M. H. Moaiyeri, A. Doostaregan and K. Navi, "Design of Energy-Efficient and Robust Ternary Circuits for Nanotechnology", Circuits, Devices & Systems, Vol. 5, No. 4, 2011, pp. 285–296.

[8] K. Navi, M. H. Moaiyeri, R. Faghih Mirzaee, O. Hashemipour, and B. Mazloom Nezhad, "Two new lowpower full adders based on majority-not gates," Elsevier, Microelectronics Journal, Vol. 40, No. 1, 2009, pp. 126-130.

[9] M. Alioto, G. Palumbo, "Analysis and comparison of the full adder block", IEEE Trans. VLSI 10 (6), 2002, pp. 806–823.

[10] M. H. Moaiyeri, R. Faghih Mirzaee, and K. Navi, "Two new low-power and high-performance full adders", Journal of Computers, Vol. 4, No. 2, 2009, pp. 119-126.

[11] A. Raychowdhury, K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design", IEEE Transactions on Nanotechnology, 4 (2) (2005) 168–179.

[12] P. Keshavarzian, K. Navi, "Efficient Carbon Nanotube Galois Field Circuit Design", IEICE, Electronics Express, 6 (9) (2009) 546-552.

[13] S. Lin, Y. B. Kim, F. Lombardi, "Design of a CNTFET-Based SRAM Cell by Dual-Chirality Selection", IEEE transaction on nanotechnology, 9 (1) (2010) 30-37.

[14] S. Lin, Y. B. Kim, F. Lombardi, "CNTFET-Based Design of ternary logic Gates and Arithmetic Circuits", IEEE Transaction on nanotechnology, 10 (2) (2011) 217-225.

[15] K. Navi, A. Momeni, F. Sharifi, P. Keshavarzian, "Two novel ultra-high speed carbon nanotube Full-Adder cells", IEICE Electron. Express, 6 (19) (2009) 1395-1401.

[16] K. Navi, M. Rashtian, A. Khatir, P. Keshavarzian, O. Hashemipour, "High Speed Capacitor-Inverter Based Carbon Nanotube Full Adder", Nanoscale Res. Lett., Springer, (2010) 859-862.

[17] S. A. Ebrahimi, P. Keshavarzian, "Ulta-Low Power and High Speed Full Adder Based-on CNTFET", European journal of Scientific Research, 2012, Vol.80 No.3, pp.358-365.